// VerilogA for ADC\_Ideal\_4bit\_FlashADC, VerilogA\_DAC\_4bit, veriloga

`include "constants.vams"

`include "disciplines.vams"

module VerilogA\_DAC\_4bit(d0,d1,d2,d3,vout,vdd,vss,vmin,vmax);

parameter real vtrans=0.5;

parameter real delay = 0;

parameter real ttime = 1p;

inout vdd,vss;

input d0,d1,d2,d3;

input vmin, vmax;

output vout;

electrical vout,vdd,vss,d0,d1,d2,d3,vmin,vmax;

real result,d\_0,d\_1,d\_2,d\_3;

analog begin

d\_3 = V(d3)\*8;

d\_2 = V(d2)\*4;

d\_1 = V(d1)\*2;

d\_0 = V(d0)\*1;

result = ((d\_3+d\_2+d\_1+d\_0) \* ((V(vmax)-V(vmin))/(16))) + V(vmin) ;

V(vout) <+ transition(result,delay,ttime);

end

endmodule